Circuits and Systems Expositions

On the Application of Thevenin and Norton Equivalent Circuits and Signal Flow Graphs to the Small-Signal Analysis of Active Circuits

W. Marshall Leach, Jr., *Senior Member, IEEE*

Abstract— **Small-signal Thevenin and Norton equivalent circuits seen looking into each terminal of the BJT and the FET are described. The application of these circuits to writing by inspection the expressions for gain, input resistance, and output resistance of multistage amplifiers is demonstrated. The application of the circuits to the noise analysis of devices is illustrated by the calculation of the noise input voltage and current of the BJT and the noise input voltage of the MOSFET. The circuits are useful for the analysis of feedback amplifiers where Mason's signal flow graph can be used to solve the simultaneous equations that are obtained. Several examples are presented which illustrate flow-graph solutions for feedback circuits.**

I. Introduction

THE SMALL-SIGNAL analysis of electronic circuits is traditionally performed by replacing all active devices in the circuit with a small-signal model. Loop or node equations are then written and solved for the desired gain or impedance. Commonly used small-signal models for the bipolar-junction transistor (BJT) are the h-parameter (or hybrid) model, the T model, and the hybrid-π model. The latter two models are also used for the field-effect transistor (FET).

In circuits containing no more than one transistor, the analysis is usually straightforward if no more than one input loop is present. If this is not the case, a Thevenin equivalent circuit can usually be made to reduce this number to one. In circuits containing more than one transistor, the analysis can become complicated when multiloop circuits must be solved. This paper presents a systematic method by which this process can be simplified. The method is based on making Thevenin and Norton equivalent circuits looking into and out of each active device port. Once this is done, the circuit solutions can usually be written by inspection. To illustrate the procedure, several examples are given. Another useful application is the noise analysis of devices. This is illustrated with the calculation of the noise input voltage and current of the BJT and the noise input voltage of the MOSFET. Although the analysis is restricted to low-frequencies, the methods can be extended to include frequency response effects.

Feedback circuits are a special case. Several examples are presented to illustrate how solutions can be written by inspection when Mason's signal flow graph [1]–[4] is used to represent the equations. A major problem in the application of flow graphs to electronic circuit analysis can be the modeling of loading effects between stages in a circuit. When this becomes a problem here, it is circumvented by formulating the flow-graph path gains in terms of the Thevenin input voltage or the Norton input current to a stage rather than in terms of the actual input voltage or current. In this way, loading effects can be accounted for in the path gains of the flow graph.

Contemporary computer technology has had a profound effect on circuit analysis and design. A user with little understanding of the operation of a circuit can write the node equations and use a software tool to solve the resulting matrix. This might lead some to believe that the traditional discipline of circuit analysis is superfluous. However, computers do not design circuits, engineers do. The traditional analysis of a circuit provides an insight into its operation that can probably never be provided solely by a computer. Only after the serious student has mastered the traditional approaches of circuit analysis is he or she qualified to use computer tools to facilitate design. The methods of analysis presented in this paper are based on traditional approaches. It is believed that such methods lead to a better fundamental understanding of circuit operation.

II. The Small-Signal Equivalent Circuits

The small-signal T models of the BJT and the MOSFET are used in this section to develop the small-signal Thevenin and Norton equivalent circuits seen looking into each device terminal. Fig. 1(a) shows the low-frequency T model of the BJT with external Thevenin sources connected to the base and emitter inputs. The external collector circuit is not shown. The intrinsic emitter resistance is given by $r_e = V_T/I_E$, where I_E is the emitter bias current and V_T is the thermal voltage. The collector-to-emitter resistance is given by $r_o = (V_{CB} + V_A)/I_C$, where V_{CB} is the collector-to-base bias

Manuscript received June 7, 1995; revised December 25, 1995. This paper was recommended by Associate Editor T. Nishi.

The author is with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA.

Publisher Item Identifier S 1057-7122(96)08334-1.

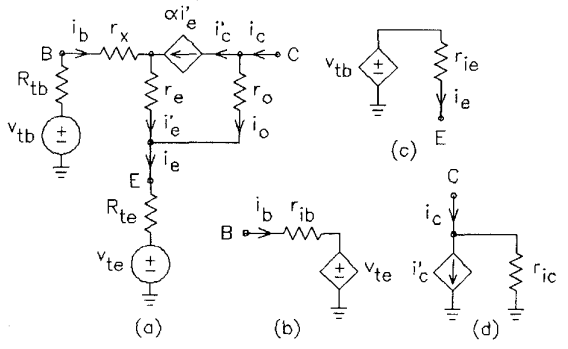


Fig. 1. (a) T model of BJT with Thevenin sources connected to base and emitter. (b) Thevenin equivalent circuit seen looking into base. (c) Thevenin equivalent circuit seen looking into emitter. (d) Norton equivalent circuit seen looking into collector.

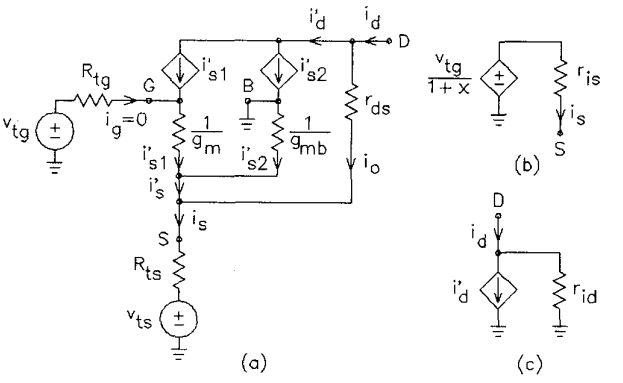


Fig. 2. (a) T model of MOSFET with Thevenin sources connected to gate and source. (b) Thevenin equivalent circuit seen looking into source. (c) Norton equivalent circuit seen looking into drain.

voltage, V_A is the Early voltage, and I_C is the collector bias current. The currents are related by $i'_c = \beta i_b = \alpha i'_e$, where $\beta = \alpha/(1-\alpha)$. Unless stated otherwise, it will be assumed that the current i_o through r_o can be neglected except when calculating the resistance seen looking into the collector, i.e., the collector output resistance.

The base voltage in Fig. 1(a) is given by $v_b = i_b r_x + i'_e r_e + i_e R_{te} + v_{te}$. When i_o is neglected, the currents are related by $i_e = i'_e = (1+\beta) i_b$. It follows that v_b can be expressed as a function of i_b and v_{te} to obtain $v_b = i_b r_{ib} + v_{te}$, where r_{ib} is the small-signal resistance seen looking into the base given by (1). It follows that the Thevenin equivalent circuit seen looking into the base consists of the resistor r_{ib} in series with the voltage v_{te}. The circuit is shown in Fig. 1(b). The emitter voltage is given by $v_e = v_{tb} - i_b(R_{tb} + r_x) - i'_e r_e$. When i_o is neglected, v_e can be expressed as a function of v_{tb} and i_e to obtain $v_e = v_{tb} - i_e r_{ie}$, where r_{ie} is the small-signal resistance seen looking into the emitter given by (2). It follows that the Thevenin equivalent circuit seen looking into the emitter consists of the resistor r_{ie} in series with the voltage v_{tb}. The circuit is shown in Fig. 1(c).

$$r_{ib} = r_x + (1+\beta)(r_e + R_{te}) \tag{1}$$

$$r_{ie} = \frac{R_{tb} + r_x}{1+\beta} + r_e. \tag{2}$$

The short-circuit collector output current $i_{c(\mathrm{sc})}$ is solved for with $v_c = 0$. When i_o is neglected, the current relations are $i_{c(\mathrm{sc})} = i'_c$, $i_b = i'_c/\beta$, and $i_e = i'_c/\alpha$. With the aid of these relations, the base-to-emitter loop equation is $v_{tb} - v_{te} = (i'_c/\beta)(R_{tb} + r_x) + (i'_c/\alpha)(r_e + R_{te})$. This equation can be solved for i'_c to obtain (3) where G_m is a transconductance given by (4).

$$i'_c = G_m(v_{tb} - v_{te}) \tag{3}$$

$$G_m = \frac{1}{(R_{tb} + r_x)/\beta + (r_e + R_{te})/\alpha}. \tag{4}$$

Alternate and useful relations for the transconductance G_m are

$$G_m = \frac{\alpha}{r_{ie} + R_{te}} = \frac{\beta}{R_{tb} + r_{ib}}. \tag{5}$$

With $v_{tb} = v_{te} = 0$, the collector output resistance is given by $r_{ic} = v_c/i_c$. To solve for this, the circuit seen looking up into r_e from the emitter node in Fig. 1(a) can be replaced by the resistor r_{ie} given by (2) to signal ground. The collector voltage can then be written $v_c = i_o(r_o + r_{ie} \,||\, R_{te})$, where $i_o = i_c - \alpha i'_e$ and $i'_e = -i_o R_{te}/(r_{ie} + R_{te})$. These equations can be solved for r_{ic} to obtain

$$r_{ic} = \frac{r_o + r_{ie} \,||\, R_{te}}{1 - G_m R_{te}} \tag{6}$$

where the first relation in (5) has been used in the denominator. The Norton equivalent circuit seen looking into the collector consists of the current i'_c given by (3) in parallel with the resistor r_{ic}. The circuit is given in Fig. 1(d). Note the effect of positive feedback in (6) which predicts that $r_{ic} \to \infty$ if $G_m R_{te} \to 1$.

Fig. 2(a) shows the low-frequency T model of the MOSFET with Thevenin sources connected to the gate and source inputs. The external drain circuit is not shown. In MOSFET circuits, the body (or bulk) is usually connected either to the source or to signal ground. Fig. 2(a) shows the body connected to signal ground. In the following, it is shown how the equations derived for this connection can be modified for the case where the body is connected to the source. The MOSFET transconductances are given by $g_m = 2\sqrt{K I_D}$ and $g_{mb} = \chi g_m$, where K is the transconductance parameter, I_D is the drain bias current, and χ is the rate of change of threshold voltage with source-to-body voltage. The transconductance parameter is given by $K = K_0(1 + \lambda V_{\mathrm{DS}})$, where V_{DS} is the drain-to-source bias voltage, λ is the channel length modulation parameter, and K_0 is the zero-bias value of K. The small-signal drain-to-source resistance is given by $r_{\mathrm{ds}} = (V_{\mathrm{DS}} + 1/\lambda)/I_D$. The parameter χ is referred to here as the transconductance ratio. It is given by $\chi = 0.5\gamma/\sqrt{\Phi + V_{\mathrm{SB}}}$, where γ is the body threshold parameter, Φ is the surface potential, and V_{SB} is the source-to-body bias voltage. Unless stated otherwise, it will be assumed that the current i_o through r_{ds} can be neglected except when calculating the resistance seen looking into the drain, i.e., the drain output resistance.

For the case $\chi = 0$, the branch in Fig. 2(a) with resistance $1/g_{mb}$ becomes open circuited. In this case, the circuit reduces to the T model for the case where the body is connected to the source. It follows that any equation derived from the circuit of

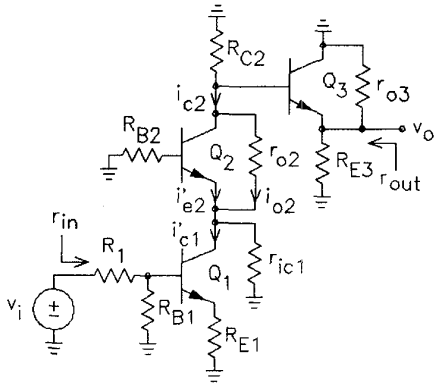


Fig. 3. Example three-stage amplifier.

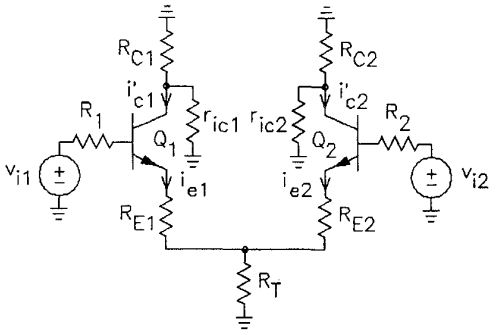


Fig. 4. Example differential amplifier.

Fig. 2(a) can be converted into a corresponding equation for the case where the body is connected to the source simply by setting $\chi = 0$ in the equation. Because the T model for the JFET is the same as the T model for the MOSFET for the case where the body is connected to the source, the equations for the JFET are also obtained by setting $\chi = 0$.

Because the FET gate current is zero, the equivalent circuit seen looking into the gate is an open circuit. The development of the small-signal Thevenin equivalent circuit seen looking into the source and the small-signal Norton equivalent circuit seen looking into the drain follow the derivations for the BJT and will not be given. The circuits are given in Fig. 2(b) and (c), where

$$r_{is} = \frac{1}{(1+\chi)g_m} \tag{7}$$

$$i'_d = G_m\left(\frac{v_{tg}}{1+\chi} - v_{ts}\right) \tag{8}$$

$$G_m = \frac{1}{r_{is} + R_{ts}} \tag{9}$$

$$r_{id} = \frac{r_{\rm ds} + r_{is} \,||\, R_{ts}}{1 - G_m R_{ts}}. \tag{10}$$

The approximations described above involving resistors r_o and $r_{\rm ds}$ force the BJT and the FET to be unilateral devices. If the BJT emitter and the FET source are connected to signal ground, the circuits become exact. When this is not the case, the resulting error can be quite small. For example, it can be shown that the percent error in calculating $i_{c(\rm sc)}$ for a BJT CE amplifier with $I_C = 1$ mA, $\beta = 100$, $R_{tb} = r_x = 0$, $R_{te} = 1$ kΩ, and $r_o = 10$ kΩ is only 0.34% when the current through r_o is neglected. For the CB amplifier with the same parameters, the percent error is 0.49%. The percent error in calculating $i_{d(\rm sc)}$ for a MOSFET CS amplifier with $K = 0.001$ A/V^2, $\chi = 0$, $R_{ts} = 1$ kΩ, $r_{\rm ds} = 30$ kΩ, and $I_D = 1$ mA is 1.1% when the current through $r_{\rm ds}$ is neglected.

The approximations involving r_o and $r_{\rm ds}$ can be avoided if these resistors are considered to be parts of the external circuits. In this case, the resistors do not appear in Figs. 1 and 2 and the circuits must be analyzed, in general, as feedback circuits. In the examples given in the following, both methods for treating r_o and $r_{\rm ds}$ are illustrated.

III. Example Analyses of Circuits without Feedback

Fig. 3 shows the signal circuit of a BJT cascode amplifier driving a common-collector stage. It is assumed that the dc bias currents and voltages are known. The collector output resistance for Q_1 is modeled as the external resistor r_{ic1} to signal ground given by (6), where $R_{tb1} = R_{B1} \,||\, R_1$ and $R_{te1} = R_{E1}$. The collector-to-emitter resistances of Q_2 and Q_3 are shown as the external resistors r_{o2} and r_{o3}.

The Norton equivalent circuit seen looking into the collector of Q_2 consists of the current $i_{c2(\rm sc)}$ in parallel with the resistor r_{ic2}, where r_{ic2} is given by (6) with $R_{tb2} = R_{B2}$ and $R_{te2} = r_{ic1}$. The current $i_{c2(\rm sc)}$ is calculated with the collector of Q_2 connected to signal ground. It is given by $i_{c2(\rm sc)} = \alpha_2 i'_{e2} + i_{o2}$. Current divider relations can be used to write $i'_{e2} = i'_{c1}(r_{ic1} \,||\, r_{ie2} \,||\, r_{o2})/r_{ie2}$ and $i_{o2} = i'_{c1}(r_{ic1} \,||\, r_{ie2} \,||\, r_{o2})/r_{o2}$, where $i'_{c1} = G_{m1} v_{tb1}$. Note that a feedback loop through r_{o2} is broken by solving for the short-circuit current $i_{c2(\rm sc)}$ rather than i_{c2}. (For an alternate solution, r_{o2} can be replaced by the resistor r_{ic2} from the collector of Q_2 to signal ground. This approximation gives $i_{c2(\rm sc)} = \alpha_2 i'_{c1}$).

The Thevenin equivalent circuit seen looking out of the base of Q_3 consists of the voltage $v_{tb3} = -i_{c2(\rm sc)}(r_{ic2} \,||\, R_{C2})$ in series with the resistance $R_{tb3} = r_{ic2} \,||\, R_{C2}$. A Thevenin equivalent circuit looking into the emitter of Q_3 can be used to solve for v_o. This is given by $v_o = v_{tb3}(r_{o3} \,||\, R_{E3})/[r_{ie3} + r_{o3} \,||\, R_{E3}]$.

The voltage gain of the circuit can be written as the product of terms

$$\begin{aligned}\frac{v_o}{v_i} &= \frac{v_{tb1}}{v_i} \times \frac{i'_{c1}}{v_{tb1}} \times \frac{i_{c2(\rm sc)}}{i'_{c1}} \times \frac{v_{tb3}}{i_{c2(\rm sc)}} \times \frac{v_o}{v_{tb3}} \\ &= \frac{R_{B1}}{R_1 + R_{B1}} \times G_{m1} \times \left[(r_{ic1} \,||\, r_{ie2} \,||\, r_{o2})\left(\frac{\alpha_2}{r_{ie2}} + \frac{1}{r_{o2}}\right)\right] \\ &\quad \times (-r_{ic2} \,||\, R_{C2}) \times \frac{r_{o3} \,||\, R_{E3}}{r_{ie3} + r_{o3} \,||\, R_{E3}}.\end{aligned} \tag{11}$$

The input and output resistances are given by $r_{\rm in} = R_1 + R_{B1} \,||\, r_{ib1}$ and $r_{\rm out} = r_{o3} \,||\, R_{E3} \,||\, r_{ie3}$. For an alternate solution, v_o/v_{tb3} can be written $v_o/v_{tb3} = (i'_{c3}/v_{tb3}) \times (i'_{e3}/i'_{c3}) \times (v_o/i'_{e3}) = G_{m3} \times (1/\alpha_3) \times (r_{o3} \,||\, R_{E3})$, where $R_{te3} = r_{o3} \,||\, R_{E3}$. When the first relation in (5) is used for G_{m3}, this solution reduces to that given in (11).

Fig. 4 shows the signal circuit of a BJT differential amplifier. The collector output resistances are modeled as external

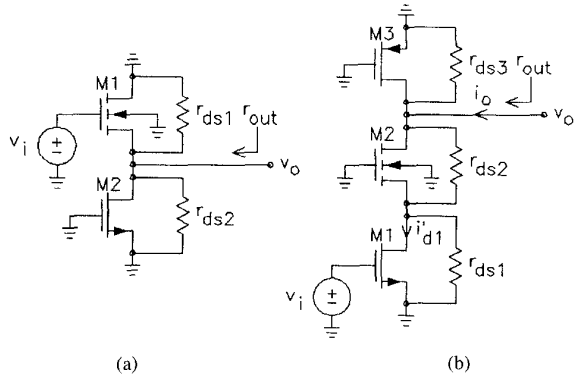


Fig. 5. (a) Example common-drain amplifier. (b) Example cascode amplifier.

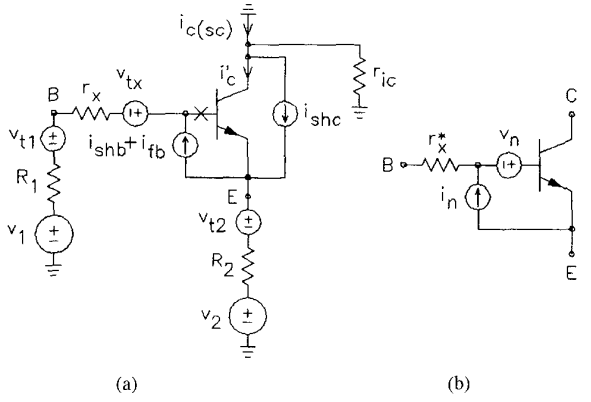


Fig. 6. (a) BJT with noise sources. (b) $V_n - I_n$ noise model of BJT, where r_x^* is a noiseless resistor.

resistors to signal ground. The Thevenin equivalent circuit seen looking into the emitter of $Q_1\,(Q_2)$ consists of the voltage $v_{i1}\,(v_{i2})$ in series with the resistance $r_{ie1}\,(r_{ie2})$, where $r_{ie1}\,(r_{ie2})$ is calculated with $R_{tb1} = R_1\,(R_{tb2} = R_2)$. Superposition can be used to solve for the emitter current in Q_1 to obtain

$$i_{e1} = \frac{v_{i1}}{r_{ie1} + R_{E1} + R_T \,||\, (R_{E2} + r_{ie2})} - \frac{v_{i2}}{r_{ie2} + R_{E2} + R_T \,||\, (R_{E1} + r_{ie1})} \times \frac{R_T}{R_T + R_{E1} + r_{ie1}} \tag{12}$$

where the latter term is a current-divider ratio. The emitter current in Q_2 is obtained by interchanging the subscripts 1 and 2 in this equation. The collector current in $Q_1\,(Q_2)$ is given by $i'_{c1} = \alpha_1 i_{e1}\,(i'_{c2} = \alpha_2 i_{e2})$. To calculate the collector output resistances r_{ic1} and r_{ic2} from (6), it is necessary to specify R_{te1} and R_{te2}. These are given by $R_{te1} = R_{E1} + R_T \,||\, (R_{E2} + r_{ie2})$ and $R_{te2} = R_{E2} + R_T \,||\, (R_{E1} + r_{ie1})$.

When the output is taken from the collector of Q_1, the common-mode rejection ratio (CMRR) caused by a noninfinite tail resistance can be expressed as the ratio $i'_{c1(d)}/i'_{c1(\mathrm{cm})}$, where $i'_{c1(d)}$ is calculated with $v_{i1} = -v_{i2} = v_i/2$ and $i'_{c1(\mathrm{cm})}$ is calculated with $v_{i1} = v_{i2} = v_i$. For the case $r_{ie1} = r_{ie2} = r_{ie}$, it follows that the CMRR is given by

$$\mathrm{CMRR} = \frac{1}{2} + \frac{R_T}{r_{ie} + R_E}. \tag{13}$$

Fig. 5(a) shows the signal circuit of a MOSFET common-drain output amplifier [5]. The drain-to-source resistance of each MOSFET is modeled as an external resistor. The Thevenin equivalent circuit seen looking into the source of M_1 consists of the voltage $v_i/(1+\chi_1)$ in series with the resistance $r_{is1} = 1/[(1+\chi_1)g_{m1}]$. The voltage gain can be written by inspection to obtain

$$\frac{v_o}{v_i} = \frac{1}{1+\chi_1} \times \frac{r_{\mathrm{ds1}} \,||\, r_{\mathrm{ds2}}}{r_{is1} + r_{\mathrm{ds1}} \,||\, r_{\mathrm{ds2}}} \tag{14}$$

where the latter term is a voltage-divider ratio. The output resistance is given by $r_{\mathrm{out}} = r_{\mathrm{ds1}} \,||\, r_{\mathrm{ds2}} \,||\, r_{is1}$. No approximations have been used in the analysis.

Fig. 5(b) shows the signal circuit of a MOSFET cascode amplifier [5]. The drain-to-source resistance of each MOSFET is modeled as an external resistor. The current i'_{d1} is given by $i'_{d1} = g_{m1} v_i$. The small-signal resistance to signal ground seen looking into the source of M_2 is $r_{is2} = 1/[(1+\chi_2)g_{m2}]$. With $v_o = 0$, the short circuit output current $i_{o(\mathrm{sc})}$ is the fraction of i'_{d1} which flows in the resistance $r_{is2} \,||\, r_{\mathrm{ds2}}$. The expression for $i_{o(\mathrm{sc})}$ is

$$i_{o(\mathrm{sc})} = g_{m1} v_i \frac{r_{\mathrm{ds1}}}{r_{\mathrm{ds1}} + r_{is2} \,||\, r_{\mathrm{ds2}}} \tag{15}$$

where the latter term is a current divider ratio. The output resistance is given by $r_{\mathrm{out}} = r_{\mathrm{ds3}} \,||\, r_{id2}$, where r_{id2} is given by (10) with $R_{ts2} = r_{\mathrm{ds1}}$. The voltage gain of the circuit is given by

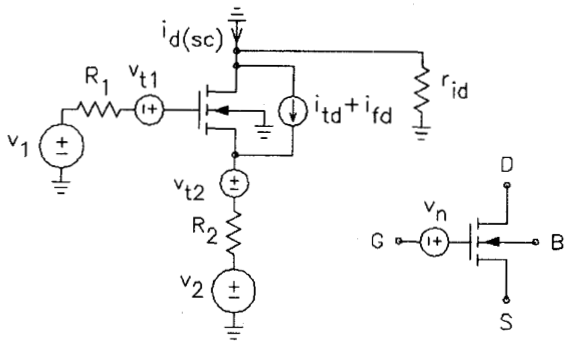
$$\frac{v_o}{v_i} = -\frac{i_{o(\mathrm{sc})} r_{\mathrm{out}}}{v_i} = -\frac{g_{m1} r_{\mathrm{ds1}}}{r_{\mathrm{ds1}} + r_{is2} \,||\, r_{\mathrm{ds2}}} \times (r_{\mathrm{ds3}} \,||\, r_{id2}). \tag{16}$$

No approximations have been used in the analysis.

IV. Example Noise Analyses

Fig. 6(a) shows a BJT with Thevenin sources connected to the base and emitter and all noise sources modeled as external sources [6]–[9]. The base spreading resistance r_x and the collector output resistance r_{ic} are modeled as external resistors. The sources v_{t1}, v_{t2}, and v_{tx}, respectively, model thermal noise generated by R_1, R_2, and r_x. The source $i_{shb} + i_{fb}$ models shot noise and flicker noise in the base bias current I_B. The source i_{shc} models shot noise in the collector bias current I_C. The mean-square values of the noise sources are given by $V_{tx}^2 = 4kTr_x\Delta f$, $I_{shc}^2 = 2qI_C\Delta f$, $I_{shb}^2 = 2qI_B\Delta f$, and $I_{fb}^2 = K_f I_B \Delta f/f$, where k is Boltzmann's constant, T is the absolute temperature, Δf is the bandwidth in Hz, q is the electronic charge, K_f is the flicker noise coefficient, and f is the frequency.

The resistor r_x is first moved to the right in Fig. 6(a) until it is at the position indicated by the X. For the equations to remain unchanged, the value of the source v_{tx} must be changed to $v_{tx} + (i_{shb} + i_{fb})r_x$. From the circuit obtained, it follows that $v_{tb} = v_1 + v_{t1} + v_{tx} + (i_{shb} + i_{fb})(R_1 + r_x)$, $R_{tb} = R_1$, $v_{te} = v_2 + v_{t2} + (i_{shc} - i_{shb} - i_{fb})R_2$, and $R_{te} = R_2$.



(a) (b)

Fig. 7. (a) MOSFET with noise sources. (b) V_n noise model of MOSFET.

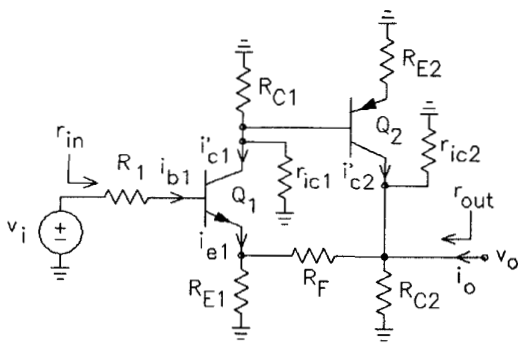


Fig. 8. Example series-shunt feedback amplifier.

The short circuit collector output current is given by $i_{c(\mathrm{sc})} = i_{shc} + G_m(v_{tb} - v_{te}) = G_m(v_1 - v_2 + v_{\mathrm{ni}})$, where v_{ni} is the noise input voltage in series with either v_1 or v_2 which generates the same noise in $i_{c(\mathrm{sc})}$. This is given by

$$v_{\mathrm{ni}} = v_{t1} - v_{t2} + v_{tx} + (i_{shb} + i_{fb})(R_1 + r_x + R_2) + i_{shc}\left(\frac{R_1 + r_x + R_2}{\beta} + \frac{r_e}{\alpha}\right). \tag{17}$$

The above equation is of the form $v_{\mathrm{ni}} = (v_{t1} - v_{t2}) + v_n + i_n(R_1 + r_x + R_2)$, where $v_n = v_{tx} + i_{shc}r_e/\alpha$ and $i_n = i_{shb} + i_{fb} + i_{shc}/\beta$. If v_{tx}, i_{shb}, and i_{shc} are assumed to be independent, it follows that the mean-square values of v_n and i_n are given by

$$V_n^2 = \langle v_n^2 \rangle = 4kTr_x\Delta f + \frac{2qV_T^2\Delta f}{I_C} \tag{18}$$

$$I_n^2 = \langle i_n^2 \rangle = 2qI_B\Delta f + \frac{2qI_C\Delta f}{\beta^2} \tag{19}$$

where the symbols $\langle\cdot\rangle$ denote a time average. The correlation coefficient between v_n and i_n is given by

$$\rho = \frac{\langle v_n i_n \rangle}{V_n I_n} = \frac{r_e\langle i_{shc}^2 \rangle}{\alpha\beta V_n I_n} = \frac{2kT\Delta f}{\beta V_n I_n}. \tag{20}$$

The noise model of the BJT is given in Fig. 6(b). The base spreading resistance r_x^* is considered to be a noiseless resistor in this model. An alternate formulation moves r_x^* into the BJT. In this case, the expressions for V_n^2 and ρ are more complicated.

Fig. 7(a) shows a MOSFET with Thevenin sources connected to the gate and source and all noise sources modeled as external sources [6]–[9]. The drain output resistance r_{id} is modeled as an external resistor. The analysis assumes the body is connected to signal ground. The transconductance ratio χ can be set to zero for the case where the body is connected to the source. The sources v_{t1} and v_{t2}, respectively, model thermal noise generated by R_1 and R_2. The source $i_{td} + i_{fd}$ models thermal noise and flicker noise generated in the channel. The mean-squared values of the noise sources are given by $I_{td}^2 = 8kTg_m\Delta f/3$ and $I_{fd}^2 = K_f I_D\Delta f/(fL^2C_{\mathrm{ox}})$, where K_f is the flicker noise coefficient, L is the effective channel length, and C_{ox} is the gate oxide capacitance per unit area.

It follows from Fig. 7(a) that $v_{tg} = v_1 + v_{t1}$, $R_{tg} = R_1$, $v_{ts} = v_2 + v_{t2} + (i_{td} + i_{fd})R_2$, and $R_{ts} = R_2$. The short circuit drain current is given by $i_{d(\mathrm{sc})} = i_{td} + i_{fd} + G_m[v_{tg}/(1+\chi) - v_{ts}]$. This can be rewritten

$$i_{d(\mathrm{sc})} = G_m\left[\frac{v_1 + v_{t1}}{1+\chi} - v_2 - v_{t2} + \frac{i_{td} + i_{fd}}{(1+\chi)g_m}\right]. \tag{21}$$

It can be seen that the noise input voltage in series with v_1 is different from the noise input voltage in series with v_2 unless $\chi = 0$, or equivalently the body is connected to the source. If the noise is reflected to the gate, the noise input voltage is given by

$$v_{\mathrm{ni}} = v_{t1} - v_{t2}(1+\chi) + \frac{i_{td} + i_{fd}}{g_m}. \tag{22}$$

This equation is of the form $v_{\mathrm{ni}} = v_{t1} - v_{t2}(1+\chi) + v_n$, where $v_n = (i_{td} + i_{fd})/g_m$. If i_{td} and i_{fd} are assumed to be independent, the mean-square value of v_n is given by

$$V_n^2 = \langle v_n^2 \rangle = \frac{4kT\Delta f}{3\sqrt{KI_D}} + \frac{K_f\Delta f}{4KfL^2C_{\mathrm{ox}}}. \tag{23}$$

The noise model for the MOSFET is given in Fig. 7(b).

V. Example Analyses of Circuits with Feedback

When the methods described above are applied to feedback amplifiers, simultaneous equations are obtained. Mason's signal flow graph is a useful tool in solving such equations. The general expression for the transmission gain T from any source node in a flow graph to any nonsource node is [3]

$$T = \frac{1}{\Delta}\sum_k P_k\Delta_k \tag{24}$$

where P_k is the gain of the kth forward path, Δ is the determinant of the graph, and Δ_k is the determinant of that part of the graph not touching the kth forward path. The determinant is given by

$$\Delta = 1 + \sum_r\left[(-1)^r\sum_m L_m^{(r)}\right] \tag{25}$$

where $L_m^{(r)}$ is the product of the loop gains of the mth possible combination of r nontouching loops.

Fig. 8 shows the signal circuit of a BJT series-shunt feedback amplifier. The collector output resistances for Q_1 and

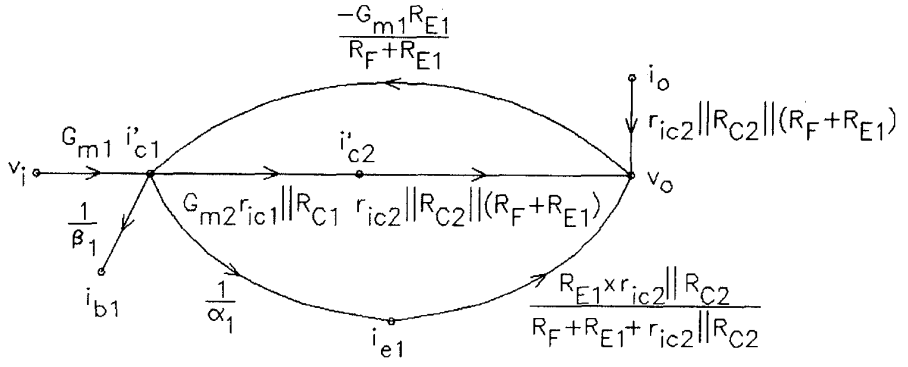


Fig. 9. Flow graph for series-shunt amplifier.

Q_2 are modeled as external resistors to signal ground. The following equations can be written

$$v_o = (i'_{c2} + i_o)[r_{ic2} \,||\, R_{C2} \,||\, (R_F + R_{E1})] + i_{e1}\frac{R_{E1}(r_{ic2} \,||\, R_{C2})}{R_{E1} + R_F + r_{ic2} \,||\, R_{C2}} \tag{26}$$

$$i'_{c2} = -G_{m2}\big[-i'_{c1}(r_{ic1} \,||\, R_{C1})\big] \tag{27}$$

$$i_{e1} = i'_{c1}/\alpha_1 \tag{28}$$

$$i'_{c1} = G_{m1}\left(v_i - v_o\frac{R_{E1}}{R_F + R_{E1}}\right) \tag{29}$$

$$i_{b1} = i'_{c1}/\beta_1 \tag{30}$$

where $R_{tb1} = R_1$, $R_{te1} = R_{E1} \,||\, R_F$, $R_{tb2} = r_{ic1} \,||\, R_{C1}$, and $R_{te2} = R_{E2}$. The minus sign precedes G_{m2} in (27) because i'_{c2} is labeled flowing out of the collector of a PNP transistor. Note that every unknown is defined by an equation, where v_i and i_o are considered to be independent variables.

A possible point of confusion in writing the equations is the determination of R_{tb} and R_{te}. In Fig. 8, for example, R_{tb1} is clearly equal to R_1. However, R_{te1} is not so clear. The correct value for R_{te1} is obtained by setting to zero all variables used in the superposition for v_{te1}. It follows from (29) that v_o is set equal to zero so that $R_{te1} = R_{E1} \,||\, R_F$. An alternate solution is to write $v_{te1} = i'_{c2}R_{E1}(r_{ic2} \,||\, R_{C2})/(R_{E1} + R_F + r_{ic2} \,||\, R_{C2})$. In this case, $R_{te1} = R_{E1} \,||\, (R_F + r_{ic2} \,||\, R_{C2})$. This solution has not been used here because it leads to a loop-gain transfer function that is not in the standard form for the shunt sampling topology. In summary, the variables used in the superposition for v_{tb} and v_{te} are set to zero in solving for R_{tb} and R_{te}.

Fig. 9 shows the flow graph for the equations. There are two forward paths from v_i to v_o, one forward path from v_i to i_{b1}, one forward path from i_o to v_o, and two loops which touch. All forward paths touch both loops so that $\Delta_k = 1$ for each forward path. The determinant is given by

$$\Delta = 1 - \left(\frac{-G_{m1}R_{E1}}{R_F + R_{E1}}\right) \times \left[G_{m2}(r_{ic1} \,||\, R_{C1})[r_{ic2} \,||\, R_{C2} \,||\, (R_F + R_{E1})] + \frac{1}{\alpha_1} \times \frac{R_{E1}(r_{ic2} \,||\, R_{C2})}{R_F + R_{E1} + r_{ic2} \,||\, R_{C2}}\right]. \tag{31}$$

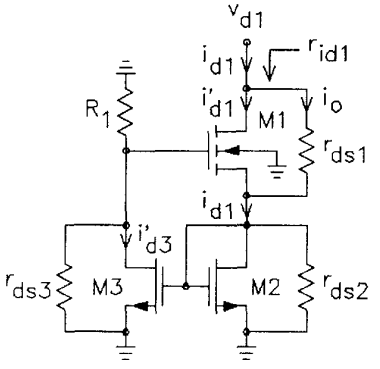


Fig. 10. MOSFET Wilson current mirror.

The voltage gain, input resistance and output resistance can be written by inspection from the flow graph to obtain

$$\frac{v_o}{v_i} = \frac{1}{\Delta} \times G_{m1} \times \left[G_{m2}(r_{ic1} \,||\, R_{C1})[r_{ic2} \,||\, R_{C2} \,||\, (R_F + R_{E1})] + \frac{1}{\alpha_1} \times \frac{R_{E1}(r_{ic2} \,||\, R_{C2})}{R_F + R_{E1} + (r_{ic2} \,||\, R_{C2})}\right] \tag{32}$$

$$r_{\text{in}} = \left(\frac{i_{b1}}{v_i}\right)^{-1} = \Delta \times \frac{\beta_1}{G_{m1}} = \Delta \times (R_1 + r_{ib1}) \tag{33}$$

$$r_{\text{out}} = \frac{v_o}{i_o} = \frac{1}{\Delta} \times [r_{ic2} \,||\, R_{C2} \,||\, (R_F + R_{E1})] \tag{34}$$

where the second expression in (5) has been used in (33). The determinant corresponds to what is commonly called the "amount of feedback" [10]. The gain is decreased by the amount of feedback, the input resistance is increased by the amount of feedback, and the output resistance is decreased by the amount of feedback. These are well-known properties of the series-shunt feedback topology.

Fig. 10 shows the signal circuit of a MOSFET Wilson current mirror [5]. The drain-to-source resistance of each MOSFET is modeled as an external resistor. The Thevenin equivalent circuit seen looking out of the source of M_1 consists of the voltage $v_{ts1} = i_o(r_{\text{ds2}} \,||\, r_{is2})$ in series with the resistance $R_{ts1} = r_{\text{ds2}} \,||\, r_{is2}$, where $r_{is2} = 1/g_{m2}$. The output resistance is given by $r_{id1} = v_{d1}/i_{d1}$. To solve for this,

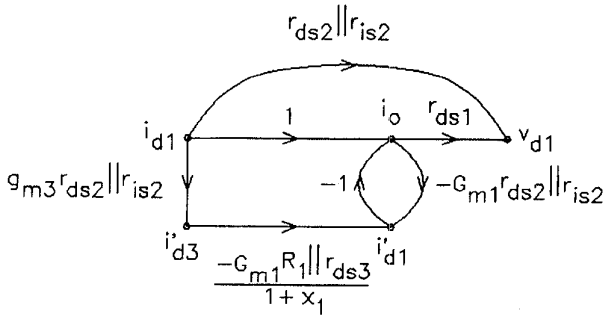


Fig. 11. Flow graph for MOSFET Wilson current mirror.

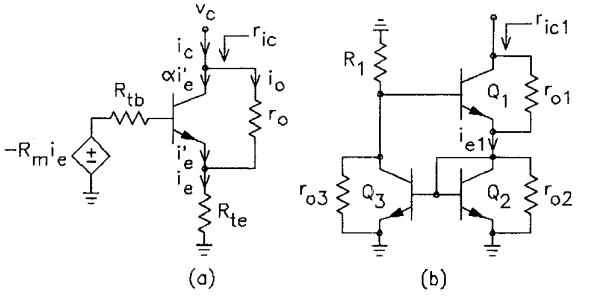


Fig. 12. (a) BJT with series sampling negative feedback. (b) BJT Wilson current mirror.

the following equations can be written

$$v_{d1} = i_o r_{ds1} + i_{d1}(r_{ds2} \,||\, r_{is2}) \tag{35}$$

$$i_o = i_{d1} - i'_{d1} \tag{36}$$

$$i'_{d1} = G_{m1}\left[-\frac{i'_{d3}(R_1 \,||\, r_{ds3})}{1+\chi_1} - i_o(r_{ds2} \,||\, r_{is2})\right] \tag{37}$$

$$i'_{d3} = g_{m3} i_{d1}(r_{ds2} \,||\, r_{is2}) \tag{38}$$

where G_{m1} is given by (9). The flow graph for the equations is given in Fig. 11. There is only one loop. There are three forward paths from i_{d1} to v_{d1}, two which touch the loop and one of which does not touch the loop. Thus $\Delta_k = \Delta$ for the latter path. The determinant is given by

$$\Delta = 1 - G_{m1}(r_{ds2} \,||\, r_{is2}). \tag{39}$$

The output resistance can be written by inspection from the flow graph to obtain

$$r_{id1} = \frac{v_{d1}}{i_{d1}} = \frac{r_{ds1}}{\Delta} \times \left[1 + g_{m3}(r_{ds2} \,||\, r_{is2}) \times \frac{G_{m1}(R_1 \,||\, r_{ds3})}{1+\chi_1}\right] + r_{ds2} \,||\, r_{is2}. \tag{40}$$

No approximations have been made in the analysis.

Fig. 12(a) shows the signal equivalent circuit of a BJT stage that occurs commonly in series-sampling feedback amplifiers. Feedback is modeled by the voltage source $-R_m i_e$, where R_m is a transresistance gain. The output resistance is given

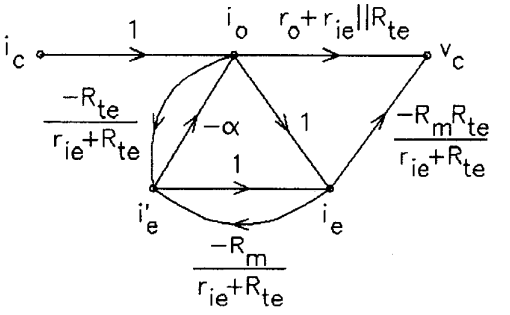


Fig. 13. Flow graph for BJT with series sampling negative feedback.

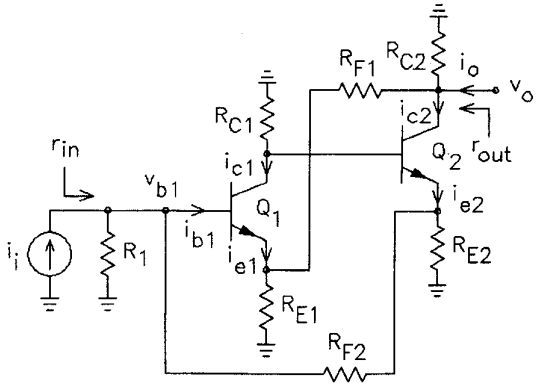


Fig. 14. Example amplifier with shunt-series and series-shunt feedback.

by $r_{ic} = v_c/i_c$. Following the derivation of (6), the following equations can be written

$$v_c = i_o(r_o + r_{ie} \,||\, R_{te}) - R_m i_e \frac{R_{te}}{r_{ie}+R_{te}} \tag{41}$$

$$i_o = i_c - \alpha i'_e \tag{42}$$

$$i'_e = -i_o \frac{R_{te}}{r_{ie}+R_{te}} - \frac{R_m i_e}{r_{ie}+R_{te}} \tag{43}$$

$$i_e = i_o + i'_e. \tag{44}$$

The flow graph is shown in Fig. 13. There are three touching loops. The determinant is given by

$$\Delta = 1 - \left[\frac{\alpha R_{te}}{r_{ie}+R_{te}} - \frac{R_m}{r_{ie}+R_{te}} + \frac{\alpha R_m}{r_{ie}+R_{te}}\right] = 1 - G_m(R_{te} - R_m/\beta) \tag{45}$$

where the first relation in (5) has been used in the simplification. There are three forward paths from i_c to v_c, one which touches two loops and two which touch all three loops. The output resistance is given by

$$r_{ic} = \frac{v_c}{i_c} = \frac{1}{\Delta} \times \left[(r_o + r_{ie} \,||\, R_{te})\Delta_1 + \left(1 - \frac{R_{te}}{r_{ie}+R_{te}}\right)\left(\frac{-R_m R_{te}}{r_{ie}+R_{te}}\right)\right] \tag{46}$$

where $\Delta_1 = 1 + R_m/(r_{ie} + R_{te})$. It is straightforward to show that (46) reduces to

$$r_{ic} = \frac{r_o(1 + G_m R_m/\alpha) + r_{ie} \,||\, R_{te}}{1 - G_m(R_{te} - R_m/\beta)} \tag{47}$$

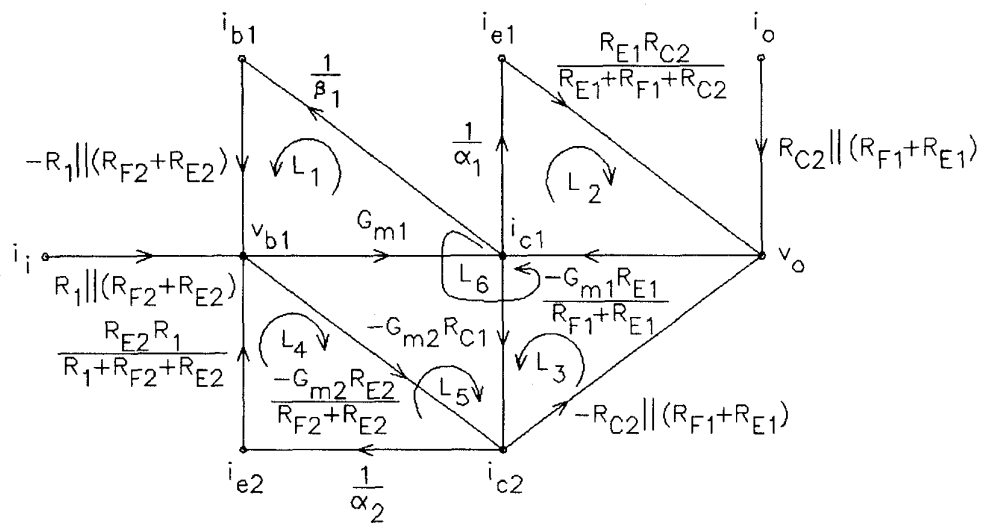


Fig. 15. Flow graph for amplifier with shunt-series and series-shunt feedback.

If $R_m = 0$, this reduces to (6). No approximations have been made in the analysis.

Fig. 12(b) shows the signal circuit of a BJT Wilson current mirror. Q_2 is connected as a diode and has the small-signal resistance $r_{ce2} = [r_{x2}/(1+\beta_2) + r_{e2}] \,||\, r_{o2}$. The output resistance of the mirror is given by (47) with r_o, G_m, α, r_{ie}, and R_{te} evaluated for Q_1, where $R_{tb1} = R_1 \,||\, r_{o3}$, $R_{te1} = r_{ce2} \,||\, r_{ib3}$, $R_m = r_{ce2}G_{m3}(R_1 \,||\, r_{o3})$, $R_{tb3} = r_{ce2}$ (calculated with $i_{e1} = 0$), and $R_{te3} = 0$. If $R_{tb1} \to \infty$, $r_{x1} = r_{x2} = r_{x3} = 0$, $r_{e3} = r_{e2}$, $r_{o2} \to \infty$, and $\beta_1 = \beta_2 = \beta_3 = \beta$, it follows that $G_{m1}R_m \to \beta^2/(2+\beta)$ and (47) reduces to

$$r_{ic1} \to r_{o1}\left(1 + \frac{\beta}{2(1+1/\beta)}\right) + \frac{r_{e2}}{2} \simeq \frac{\beta r_{o1}}{2}. \tag{48}$$

This is a well-known result for the Wilson mirror [6].

Fig. 14 shows a circuit with both series-shunt and shunt-series feedback [11]. The signal source is represented as a Norton equivalent. To simplify the equations, it will be assumed that $r_o = \infty$ for each BJT. The circuit equations are

$$v_o = (i_o - i_{c2})[R_{C2} \,||\, (R_{F1} + R_{E1})] + i_{e1}\frac{R_{E1}R_{C2}}{R_{E1}+R_{F1}+R_{C2}} \tag{49}$$

$$i_{c2} = G_{m2}\left(-i_{c1}R_{C1} - v_{b1}\frac{R_{E2}}{R_{F2}+R_{E2}}\right) \tag{50}$$

$$i_{e1} = i_{c1}/\alpha_1 \tag{51}$$

$$i_{c1} = G_{m1}\left(v_{b1} - v_o\frac{R_{E1}}{R_{F1}+R_{E1}}\right) \tag{52}$$

$$v_{b1} = (i_i - i_{b1})[R_1 \,||\, (R_{F2}+R_{E2})] + i_{e2}\frac{R_{E2}R_1}{R_1+R_{F2}+R_{E2}} \tag{53}$$

$$i_{e2} = i_{c2}/\alpha_2 \tag{54}$$

$$i_{b1} = i_{c1}/\beta_1 \tag{55}$$

where $R_{tb1} = 0$, $R_{te1} = R_{E1} \,||\, R_{F1}$, $R_{tb2} = R_{C1}$, and $R_{te2} = R_{E2} \,||\, R_{F2}$. Note that $v_{tb1} = v_{b1}$ in (52) so that v_{b1} is set to zero to solve for R_{tb1}. Also, v_{te2} in (50) is expressed as a function of v_{b1} so that v_{b1} is set to zero to solve for R_{te2}.

The flow graph for the equations is shown in Fig. 15. The graph has six loops. The loop gains are given by

$$L_1 = -G_{m1}\frac{1}{\beta_1}[R_1 \,||\, (R_{F2}+R_{E2})] \tag{56}$$

$$L_2 = -\frac{1}{\alpha_1} \times \frac{R_{E1}R_{C2}}{R_{E1}+R_{F1}+R_{C2}} \times \frac{G_{m1}R_{E1}}{R_{F1}+R_{E1}} \tag{57}$$

$$L_3 = -G_{m2}R_{C1}[R_{C2} \,||\, (R_{F1}+R_{E1})]\frac{G_{m1}R_{E1}}{R_{F1}+R_{E1}} \tag{58}$$

$$L_4 = -\frac{1}{\alpha_2} \times \frac{R_{E2}R_1}{R_1+R_{F2}+R_{E2}} \times \frac{G_{m2}R_{E2}}{R_{F2}+R_{E2}} \tag{59}$$

$$L_5 = -\frac{1}{\alpha_2} \times \frac{R_{E2}R_1}{R_1+R_{F2}+R_{E2}}G_{m1}G_{m2}R_{C1} \tag{60}$$

$$L_6 = \frac{1}{\beta_1}[R_1 \,||\, (R_{F2}+R_{E2})]\frac{G_{m2}R_{E2}}{R_{F2}+R_{E2}} \times [R_{C2} \,||\, (R_{F1}+R_{E1})]\frac{G_{m1}R_{E1}}{R_{F1}+R_{E1}}. \tag{61}$$

There is one combination of two nontouching loops L_2 and L_4. The determinant is given by

$$\Delta = 1 - (L_1 + L_2 + L_3 + L_4 + L_5 + L_6) + L_2L_4. \tag{62}$$

There are three forward paths from i_i to v_o, each of which touches all six loops. Therefore, $\Delta_k = 1$ for each path. The transresistance gain is given by

$$\frac{v_o}{i_i} = \frac{1}{\Delta} \times \left[G_{m1}\left(\frac{1}{\alpha_1} \times \frac{R_{E1}R_{C2}}{R_{E1}+R_{F1}+R_{C2}} + G_{m2}R_{C1}[R_{C2} \,||\, (R_{F1}+R_{E1})]\right) + \frac{G_{m2}R_{E2}}{R_{F2}+R_{E2}}[R_{C2} \,||\, (R_{F1}+R_{E1})]\right]. \tag{63}$$

There is only one path from i_o to v_o and it touches three of the six loops. The Δ_k for this path is $\Delta_k = 1 - (L_1 + L_4 + L_5)$.

The output resistance is given by

$$r_{\text{out}} = \frac{v_o}{i_o} = \frac{1-(L_1+L_4+L_5)}{\Delta}[R_{C2} \,||\, (R_{F1}+R_{E1})]. \tag{64}$$

There is one path from i_i to v_{b1} which touches four of the six loops. The Δ_k for this path is $\Delta_k = 1-(L_2+L_3)$. The input resistance is given by

$$r_{\text{in}} = \frac{v_{b1}}{i_i} = \frac{1-(L_2+L_3)}{\Delta}[R_1 \,||\, (R_{F2}+R_{E2})]. \tag{65}$$

If $R_{F1} \to \infty$, the circuit becomes a familiar shunt-series feedback amplifier. In this case, $L_2 = L_3 = L_6 = 0$ and the expression for Δ is simplified a great deal. For the shunt-series topology, the circuit gain is commonly expressed as a current gain, where the output current is i_{c2}, i.e., the current in R_{C2}. For $R_{F1} \to \infty$, the current gain is given by

$$\frac{i_{c2}}{i_i} = \frac{1}{\Delta} \times [R_1 \,||\, (R_{F2}+R_{E2})] \times \left[-G_{m1}G_{m2}R_{C1} - \frac{G_{m2}R_{F2}}{R_{F2}+R_{E2}}\right]. \tag{66}$$

The resistance seen looking into the collector of Q_2 is infinite because of the assumption that $r_{o2} = \infty$. For $r_{o2} < \infty$ and $R_{F1} \to \infty$, r_{ic2} can be calculated from (47). In this case, G_{m2} and r_{ie2} in (47) must be calculated with $R_{tb2} = R_{C1}$ and $R_{te2} = R_{E2} \,||\, [R_{F2}+(R_1 \,||\, r_{ib1})]$, where r_{ib1} is calculated with $R_{te1} = R_{E1}$. The expression for R_m in (47) is

$$R_m = \frac{v_{b1}}{i_{e2}} \times \frac{i_{c1}}{v_{b1}} \times \frac{v_{tb2}}{i_{c1}} = \frac{R_{E2}(R_1 \,||\, r_{ib1})}{R_{E2}+R_{F2}+(R_1 \,||\, r_{ib1})} \times G_{m1} \times (-R_{C1}) \tag{67}$$

where G_{m1} and r_{ib1} are calculated with $R_{tb1} = 0$ and $R_{te1} = R_{E1}$.

VI. Conclusion

The expressions for the small-signal gain, input resistance, and output resistance of active circuits can often be written by inspection if the small-signal Thevenin and Norton equivalent circuits seen looking into each terminal of the active devices are known. These circuits can also be used to simplify the noise analysis of active devices. In the analysis of circuits with feedback, simultaneous equations must be solved. Mason's signal flow graph is a convenient tool for obtaining the solution.

References

[1] S. J. Mason, "Feedback theory—Some properties of signal flow graphs," *IRE Proc.*, vol. 41, pp. 1144–1156, Sept. 1953.

[2] ——, "Feedback theory—Further properties of signal flow graphs," *IRE Proc.*, vol. 44, pp. 920–926, July 1956.

[3] S. J. Mason and H. J. Zimmermann, *Electronic Circuits, Signals, and Systems*. New York: Wiley, 1960.

[4] J. Choma, Jr., "Signal flow analysis of feedback networks," *IEEE Trans. Circuits Syst.*, vol. 37, pp. 455–463, Apr. 1990.

[5] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*. New York: Holt, Rinehart, and Winston, 1987.

[6] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. New York: Wiley, 1993.

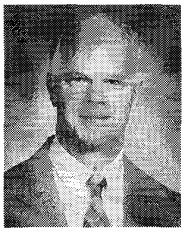
[7] H. W. Ott, *Noise Reduction Techniques in Electronic Systems*, 2nd ed. New York: Wiley, 1988.

[8] C. D. Motchenbacher and J. A. Connelly, *Low-Noise Electronic System Design*. New York: Wiley, 1993.

[9] W. M. Leach, Jr., "Fundamentals of low-noise analog circuit design," *IEEE Proc.*, vol. 82, pp. 1515–1538, Oct. 1994.

[10] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*. Philadelphia, PA: Saunders, 1991.

[11] K. H. Chan and R. G. Meyer, "A low-distortion monolithic wide-band amplifier," *IEEE J. Solid-State Circuits*, vol. SC-12, pp. 685–690, Dec. 1977.



W. Marshall Leach, Jr. (S'63–M'64–SM'82) received the B.S. and M.S. degrees in electrical engineering from the University of South Carolina, Columbia, in 1962 and 1964, respectively, and the Ph.D. degree in electrical engineering from the Georgia Institute of Technology, Atlanta, in 1972.

In 1964, he was with the National Aeronautics and Space Administration, Hampton, VA. From 1965 to 1968, he served as an officer in the U.S. Air Force. Since 1972, he has been a faculty member of the Georgia Institute of Technology, where he is presently Professor with the School of Electrical and Computer Engineering. His interests are electronic design and applications, electroacoustic modeling, and applied electromagnetics.

Dr. Leach is a fellow of the Audio Engineering Society and a member of the Acoustical Society of America.